REMARKS

Claims 1-3, 6, 8-14 and 16 have been amended. Claims 7, 15 and 17-19 have been canceled. Claim 20 is newly presented. Claims 1-6, 8-14, 16 and 20 remain pending. No new matter has been added.

Drawing Objection

Figure 1 stands objected to for lacking "Prior Art" label. Figure 1 has been amended to include a "Prior Art" label, and the corrected drawing is included in this response. Withdrawal of the drawing objection is requested.

Claim Objections

Claim 19 stands objected to for lacking of antecedent basis. Claim 19 has been canceled thereby rendering the objection to claim 19 moot. Withdrawal of the claim objection is requested.

Rejection under 35 U.S.C. 102(b)

Claims 1-6, 8-14 and 16-19 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,218,876, issued on April 17, 2001, to Sung et al (Sung). Under 35 U.S.C. 102(b), a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.

Amended, claim 1 is drawn to a circuit comprising:

> a first phase-locked loop to receive a first reference signal and a first feedback signal, and to produce a data clock signal having a first frequency based at least in part upon the first reference signal and a first feedback signal; and

> a second phase-locked loop coupled to the first phase-locked loop by a first signal path, the second phase-locked loop to receive a second reference signal on the first signal path and a second feedback signal on a second signal trace and to produce a second clock signal having a second frequency based at least in part upon the second reference signal and the second feedback signal, the first feedback signal and the second reference signal being derived from the data clock signal and the second feedback signal being derived from the second clock signal, wherein the second reference signal and the second feedback signal have equivalent signal distribution delays.

Thus, in at least one embodiment as reflected in claim 1, the signal distribution delays of the second reference signal and the second feedback signal of the second phase-locked loop are designed to be equivalent. For example, in Applicant's Figure 4, the second reference signal (e.g., represented by signal path 411) and the second feedback signal (e.g., represented by signal path 415) would have equivalent signal distribution delays in order e.g. to provide first-order common mode tracking (as described on page 9, lines 1-6 of Applicant's specification). Sung fails to teach or otherwise suggest that the first phase-locked loop and the second phase-locked loop are connected by a first signal path, and the second feedback signal is provided on a second signal path, where the second reference signal and the second feedback signal have equivalent signal distribution delays.

For at least this reason, Applicant submits that claim 1 is not anticipated by Sung and requests that claim 1 be allowed. Given that claims 2-6 and 8 depend from claim 1, Applicant submits that claims 2-6 and 8 are allowable for at least the same reasons as claim 1.

Amended claim 9 is drawn to a processor comprising:

> a processing core;
> input-output circuitry;
> a first phase-locked loop coupled to the input-output circuitry by a first signal trace, the first phase-locked loop producing a first output signal having a first frequency based at least in part upon a first reference signal and a first feedback signal derived from the first output signal, and providing the first output signal as a data clock signal to the input-output circuitry on the first signal trace; and
> a second phase-locked loop coupled to the first phase-locked loop by a second signal trace and to the processor core circuitry by a third signal trace, the second phase-locked loop providing a second output clock signal to the processor core circuitry on the third signal trace, the second output signal having a second frequency based at least in part upon a second reference signal provided by the second signal trace and derived from the first output signal and a second feedback signal derived from the second output signal.

Thus, ***a processor*** includes a processing core, input-output (I/O) circuitry, and a first and second cascaded phase-locked loops (PLLs) where the first PLL provides a first clock signal to the I/O circuitry on a first signal trace and the second PLL provides a second clock signal to the processing core on a second signal trace.

Sung fails to teach or suggest that ***within a processor*** the first phase-locked loop is coupled to an **input-output circuitry *of the processor*** via a first signal trace, and the second phase-locked loop is coupled to core circuitry via a second signal trace. Instead, Sung merely discloses two phase-locked loops arranged in series, where either the first or second PLL may provide an output signal to I/O registers of to programmable logic (see e.g., figure 4). Although Figure 5 illustrates a data processing system including I/O 308, PLD 10, and processor 304, Applicant submits that Sung does not describe or otherwise suggest that the first and second cascaded PLLs are located ***within the processor***. Moreover, the PLD and I/O components illustrated in

Figures 1 and 4 of Sung are clearly illustrated as being independent from processor 304. Applicant respectfully submits that claim 9 is not anticipated by Sung.

As claims 10-14, 16 and 20 are dependent on Claim 9, Applicant submits that these claims are patentable over Sung for at least the above-stated reasons and are further distinguished by additional elements recited therein.

Rejection of Claim 31 under 35 U.S.C. 103(a)

Claims 7 and 15 stand rejected under 35 U.S.C. 103(a) over Sung. Claims 7 and 15 have been canceled thereby rendering the rejection to these claims as moot. Notwithstanding their cancellation, Applicant respectfully disagrees with Examiners characterization of claims 7 and 15. In particular, the selection of the different bandwidth is important in the operation of the cascaded phase-locked loops. For example, in certain designs, if the bandwidth of the second phase-locked loop is smaller then three times of the first, the cascaded phase-locked loop might become unstable.

Claims 1-14, 16 and 20 are believed to be in condition for allowance. Entry of the foregoing amendments is requested and a Notice of Allowance is earnestly solicited. Please contact the undersigned at regarding any questions or concerns associated with the present matter.

Respectfully submitted,
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